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Appl. No. 10/730,834
Reply to Office action of January 24, 2007

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Amendments to the Claims:

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

- 5 1. (currently amended) A chip comprising:
- a silicon semiconductor substrate;
 - a MOS device on a surface of said silicon substrate;
 - a metallization structure over said silicon semiconductor substrate, wherein said
10 metallization structure comprises a first patterned circuit layer and a second patterned
circuit layer over said first patterned circuit layer;
 - a dielectric layer between said first and second patterned circuit layers;
 - a passivation layer over said metallization structure, over said first and second
15 patterned circuit layers and over said dielectric layer, wherein an opening in said
passivation layer exposes a top surface of said metallization structure, wherein said
passivation layer comprises a nitride layer and an oxide layer; and
 - a third patterned circuit layer comprising a first portion connected to said top
20 surface through said opening and used to have a metal bump formed thereover, a
second portion used to be in contact with a testing probe, and a third portion used to
be wirebonded thereto, wherein said first portion is connected to said second portion.
- 20 Claim 2 (canceled)
- 25 3. (previously presented) The chip of Claim 1, wherein said second portion comprises
a gold layer having a thickness of greater than 1 micron.
- 30 Claim 4 (canceled)
5. (currently amended) The chip of Claim 1, wherein said third patterned circuit layer
comprises a gold layer and a nickel layer under said gold layer.